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FAIRCHILD SEMICONDUCTOR CORPORATION

UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR, INC., a California corporation; and ALPHA & OMEGA SEMICONDUCTOR, LTD., a Bermuda corporation,

Plaintiffs and Counterdefendants,

v.

FAIRCHILD SEMICONDUCTOR CORP., a Delaware corporation,

Defendant and Counterclaimant.

AND RELATED COUNTERCLAIMS.

Case No. C 07-2638 JSW (EDL)
(Consolidated with Case No. C 07-2664 JSW)

DECLARATION OF DR. RICHARD A. BLANCHARD IN SUPPORT OF FAIRCHILD'S OPPOSITION TO PLAINTIFFS' MOTION TO STRIKE FAIRCHILD'S PATENT LOCAL RULE 3-1 DISCLOSURE

DATE: December 11, 2007
TIME: 9:00 a.m.
COURTROOM: Hon. Elizabeth D. Laporte

I, Dr. Richard A. Blanchard, declare as follows:

1. I have been retained as an expert regarding semiconductor technology by Defendant and Counterclaimant Fairchild Semiconductor, Corporation ("Fairchild"). This Declaration is submitted in support of Fairchild's Opposition to the Motion of Alpha & Omega Semiconductor, Inc., and Alpha & Omega Semiconductor, Ltd., (collectively, "AOS") to Strike Fairchild's Patent Local Rule 3-1 Disclosure. I have personal knowledge of the matters stated herein and if called to testify as a witness, I could and would competently testify thereto.

2. I received a BSEE degree in 1968 and an MSEE degree in 1970 from MIT, and a Ph.D in Electrical Engineering from Stanford University in 1982. I was an Associate Professor, Assistant Division Chairman of the Engineering & Technology Division at Foothill College from 1974 to 1978, where among other things, I developed the curriculum for the Semiconductor Technology Program.

3. I have over 35 years of experience in the semiconductor and electronics industries. I am currently employed as the Director of Advanced Technologies at the Silicon Valley Expert Witness Group, Inc. ("SVEWG") and have extensive consulting experience since 1998 for SVEGW. Prior to working for SVEGW, I was Principal Engineer and Division Manager of the Electrical/Electronic Division of Failure Analysis (Exponent) Associates, Inc., from 1991 to 1998. As Division Manager, my duties included failure analysis and reverse engineering of solid-state electronic components and circuits, failure analysis of electric and electronic systems, subsystems, and components, and consulting with respect to Power MOS and Smart Power Technologies. Prior to that, I was employed by IXYS Corporation from 1987-1991, by Siliconix, Inc., from 1982-1987, by Supertex, Inc., from 1976-1982, by Cognition, Inc., from 1976 to 1978, by Foothill College from 1974-1978, as an independent consultant to the semiconductor industry from 1974-1976 and by Fairchild Semiconductor from 1970-1974.

4. I have testified in court and in deposition on numerous occasions as an expert witness, and I have served as an arbitrator and as a court-appointed special master. I have published several books and numerous articles on semiconductor design and process development, as well as failure analysis. I hold more than 130 U.S. patents on semiconductor technology. I am a member of the IEEE, the Electrostatic Discharge Society, and the International Microcircuits and Packaging Society.

5. I have reviewed Fairchild's Disclosure of Asserted Claims and Preliminary Infringement Contentions ("PICs") dated August 31, 2007. The PICs include a claim chart analysis for 14 AOS products. The claim charts, in turn, refer to numerous figures for each product, including technical figures such as scanning electron microscopy ("SEM") images, scanning capacitance microscopy ("SCM") images, and secondary ion mass spectroscopy ("SIMS") data. Prior to the service of these PICs, I reviewed these technical figures, and I also reviewed the "MOSFET Selector Guide – All Products," which is included as Exhibit 1 in the PICs. The MOSFET Selector Guide links to datasheets for the accused AOS products that are publicly available for download at AOS's website (http://www.aosmd.com/web/home.jsp). Datasheets contain information about each product, including its operating characteristics and how it is packaged.

6. Based on my review of product information concerning the accused AOS products, all of which are vertical power MOSFETs, including AOS's datasheets and other information from AOS's website, I conclude the accused products can be categorized using four basic criteria: (1) whether they are either N-channel devices, P-channel devices, dual-channel devices, or complementary devices; (2) whether they have either a closed-cell or an open-cell configuration; (3) whether they have either a trench gate design or a planar gate design; and (4) their drain-source voltage (V_{DS}) rating.

7. An N-channel device includes one N-type transistor, which is made of one or more N-type "source regions" formed in one or more P-type "wells," which in turn are formed on one or more N-type "drain regions."[1] The device includes a single source contact, a single drain contact, and a single gate contact. When an N-type transistor is turned on, an N-type "channel" is formed at the

[1] An N-type region is made of silicon that has been doped with a Group V element (such as Phosphorus or Arsenic), whereas a P-type region is made of silicon that has been doped with a Group III element (such as Boron). Both are conductive, but an N-type region is conductive because it has a net excess of electrons, whereas a P-type region is conductive because is has a net deficit of electrons. Even though both N-type and P-type regions are conductive, current may not be able to flow from an N-type region to a P-type region, depending upon the polarity of the applied bias (voltage). This characteristic of the boundary between an N-type region and a P-type region is what enables a transistor to be turned on or off.

surface of the P-type well(s) that is adjacent to the gate between the N-type source region(s) and the N-type drain region(s), allowing current to flow between the source contact and the drain contact. Conversely, a P-channel device includes one P-type transistor, which is made of one or more P-type source regions formed in one or more N-type wells, which in turn are formed on one or more P-type drain regions. The device includes a single source contact, a single drain contact, and a single gate contact. When a P-type transistor is turned on, a P-type channel is formed at the surface of the N-type well(s) that is adjacent to the gate between the P-type source region(s) and the P-type drain region(s), allowing current to flow between the source contact and the drain contact. A dual-channel device includes either two N-type transistors or two P-type transistors, but in either case includes two source contacts, two drain contacts, and two gate contacts. A complementary device includes one N-type transistor and one P-type transistor, and includes two source contacts, two drain contacts, and two gate contacts. All of AOS's accused vertical power MOSFETs fall into one of these four categories.

8. A power MOSFET device with a trench gate design includes one or more gates formed in trenches that are etched vertically into the silicon. When a trench device is turned on by applying a voltage to the gate, current flows vertically through the channel that is formed adjacent to the vertical sides of the gate. A power MOSFET device with a planar gate design includes one or more gates that are parallel to the surface of the silicon substrate. When a planar device is turned on by applying a voltage to the gate, current flows horizontally through the channel that is formed adjacent to the bottom surface of the gate. Fairchild has accused only AOS vertical power MOSFET products that include a trench design.

9. A power trench MOSFET device with a closed-cell configuration generally includes transistor cells arranged in a grid, having MOSFET cells that are bordered on all sides by trench walls. The cells often are square or hexagonal in shape. A power trench MOSFET device with an open-cell configuration, on the other hand, generally includes cells arranged in parallel stripes, having MOSFET cells that are bordered on only two sides by trench walls. All commercial power MOSFETs have either a closed-cell design or an open-cell design.

10. The drain-source voltage (V_{DS}) of a power MOSFET is the amount of voltage that the device is rated to safely withstand.[2] In my experience, "low-voltage devices" are those having a drain-source voltage between approximately 20 and 100 V for an N-channel device, and between approximately -20 and -100 V for a P-channel device. Applying voltage greater than the rated drain-source voltage can result in current flow between the drain and the source, even if the device is turned off. This condition, called "breakdown," is highly undesirable and can result in destruction of the device.

11. The 14 AOS power MOSFET products analyzed in Fairchild's PICs include N-channel devices, P-channel devices, and dual-channel devices. In particular, AO4410, AO4422, AO4468, AO4704, AO6402, AOD414, AOL1412, AOD438, and AOL1414 are N-channel devices. AO4413A and AO6405 are P-channel devices. AO4812, AO4914, and AO4912 are dual-channel devices. The 14 AOS products also include both closed-cell and open-cell designs. AO4410, AO4413A, AO4422, AO4468, AO4704, AO4914, AO6402, AO6405, AOD414, and AOL1412 are closed-cell designs. AO4912, AOD438, and AOL1414 are open-cell designs. The 14 devices analyzed in the PICs all have a trench design. Furthermore, the 14 devices analyzed in the PICs all are low voltage devices. Of relevance to the issue of infringement of the Fairchild patents that are the subject of the PICs, each of these 14 AOS products has a similiar dopant concentration profile in a cross-section between the trenches.

12. Based on my experience in the power MOSFET industry, I conclude that it is highly likely that each of the accused AOS power MOSFETs has features similar to the 14 products analyzed in the PICs insofar as those features bear on the issue of infringement. This conclusion is based on the fact that the 14 products in the PICs share the same basic attributes and characteristics of all the other accused AOS power MOSFETs. In particular, all 342 accused products are either N-channel devices,

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[2] Voltage can be thought of as being equivalent to regions of different air pressure on a weather map. Air flows from regions of higher air pressure to regions of lower air pressure. Similarly, electric current flows from regions having a higher electrical potential to regions having a lower electrical potential.

P-channel devices, dual-channel devices, or complementary devices. They all are either closed-cell designs or open-cell designs. They all have a trench design. And importantly, they all are low-voltage devices. The only type of accused AOS power MOSFET that is not included in the 14 products analyzed in Fairchild's PICs is a complementary device. I expect, however, that a low-voltage complementary trench device would have the same dopant profile as a low-voltage N-channel trench device and a low-voltage P-channel trench device, because a complementary device is simply a package that includes both an N-channel power MOSFET transistor and a P-channel power MOSFET transistor.

13. To the extent possible, companies in the power MOSFET industry prefer to use similar processes to make devices that have similar features, because it is cost-effective to do so. Therefore, it is standard practice in the power MOSFET industry to use the same process from one product to the next for a given generation of products. Based upon the documents I have reviewed that are identified above, I believe that all of AOS's accused power MOSFET products are manufactured using processes that are the same in all respects that are relevant to the issue of infringement. My opinion is further supported by the fact that, to my knowledge, AOS has provided no facts or contentions that the 14 products analyzed in the PICs are different from the other accused products in any way that is relevant to infringement.

14. I understand that Fairchild has accused 342 AOS trench-design power MOSFET products of infringement. The issue of infringement relates to the manufacture of the silicon power MOSFET chip(s) contained in each of those products. A power MOSFET product includes one or more MOSFET chips, and possibly additional devices such as a Schottky diode, all contained in a single package. A particular power MOSFET chip may be placed in different package types to provide a customer with different products for different application requirements. In each of these examples, the power MOSFET chip itself is the same, and the infringement analysis would be the same for all products that contain the same chip. This is true even if these products have additional devices, or use different packaging, and therefore are identified with different part numbers in AOS catalogs or product literature.

15. I understand that AOS believes that Fairchild should prepare a claim chart and reverse-

engineering data for each of the 342 accused products. Based on my experience in the semiconductor industry, requiring Fairchild to perform such reverse-engineering analysis for all 342 products would be unnecessary. As I have explained above, based on the similarity of the features of all the accused products as they relate to the infringement issues in this case, little if any additional meaningful information is likely be obtained by further reverse-engineering analysis. I believe that Fairchild's PICs more than adequately support its contentions that each of the 342 accused AOS products infringes the asserted claims.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct to the best of my knowledge and belief.

Executed this 6th day of November 2007, in Mt. View, California.

By: Richard A. Blanchard
Dr. Richard A. Blanchard

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